

**NOT RECOMMENDED FOR NEW DESIGNS  
NO RECOMMENDED REPLACEMENT**  
contact our Technical Support Center at  
1-888-INTERSIL or www.intersil.com/tsc

**Dual Digitally Controlled Potentiometer (XDCP™) with Operational Amplifier**

**FEATURES**

- Two CMOS voltage operational amplifiers
- Two digitally controlled potentiometers
- Can be combined or used separately
- Amplifiers:
  - Low voltage operation
  - $V+/V- = \pm 2.7V$  to  $\pm 5.5V$
  - Rail-to-rail CMOS performance
  - 1MHz gain bandwidth product
- Digitally controlled potentiometers
  - Dual 64 tap potentiometers
  - $R_{total} = 10k\Omega$
  - 2-wire serial interface
  - $V_{CC} = 2.7V$  to  $5.5V$

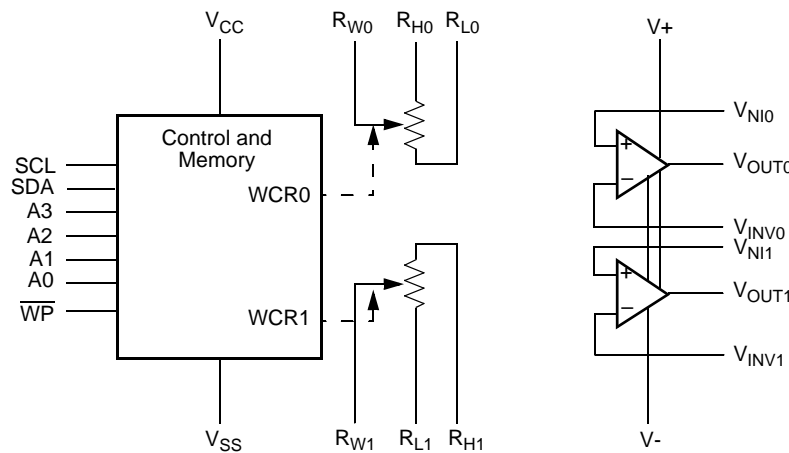
**DESCRIPTION**

The X9438 is a monolithic CMOS IC that incorporates two operational amplifiers and two nonvolatile digitally controlled potentiometers. The amplifiers are CMOS differential input voltage operational amplifiers with near rail-to-rail outputs. All pins for the two amplifiers are brought out of the package to allow combining them with the potentiometers, or using them as complete stand-alone amplifiers.

The digitally controlled potentiometers consist of a series string of 63 polycrystalline resistors that behave as standard integrated circuit resistors. The two-wire serial port, common to both pots, allows the user to program the connection of the wiper output to any of the resistor nodes in the series string. The wiper position is saved in the on board E2 memory to allow for nonvolatile restoration of the wiper position.

A wide variety of applications can be implemented using the potentiometers and the amplifiers. A typical application is to implement the amplifier as a wiper buffer in circuits that use the potentiometer as a voltage reference. The potentiometer can also be combined with the amplifier yielding a digitally programmable gain amplifier or programmable current source.

**BLOCK DIAGRAM**



**PIN DESCRIPTIONS**

**Host Interface Pins**

**Serial Clock (SCL)**

The SCL input is used to clock data into and out of the X9438.

**Serial Data (SDA)**

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor.

**Device Address (A<sub>0</sub> - A<sub>3</sub>)**

The address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9438. A maximum of 16 devices may share the same 2-wire serial bus.

**Potentiometer Pins<sup>(1)</sup>**

**R<sub>H</sub> (R<sub>H0</sub> - R<sub>H1</sub>), R<sub>L</sub> (R<sub>L0</sub> - R<sub>L1</sub>)**

The R<sub>H</sub> and R<sub>L</sub> inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

**R<sub>W</sub> (R<sub>W0</sub> - R<sub>W1</sub>)**

The wiper output is equivalent to the wiper output of a mechanical potentiometer.

**Amplifier and Device Pins**

**Amplifier Input Voltage V<sub>NI(0,1)</sub> and V<sub>INV(0,1)</sub>**

V<sub>NI</sub> and V<sub>INV</sub> are inputs to the noninverting (+) and inverting (-) inputs of the operational amplifiers.

**Amplifier Output Voltage V<sub>OUT(0,1)</sub>**

V<sub>OUT</sub> is the voltage output pin of the operational amplifier.

**Hardware Write Protect Input  $\overline{WP}$**

The  $\overline{WP}$  pin, when low, prevents non-volatile writes to the wiper counter registers.

Note: (1) Alternate designations for R<sub>H</sub>, R<sub>L</sub>, R<sub>W</sub> are V<sub>H</sub>, V<sub>L</sub>, V<sub>W</sub>

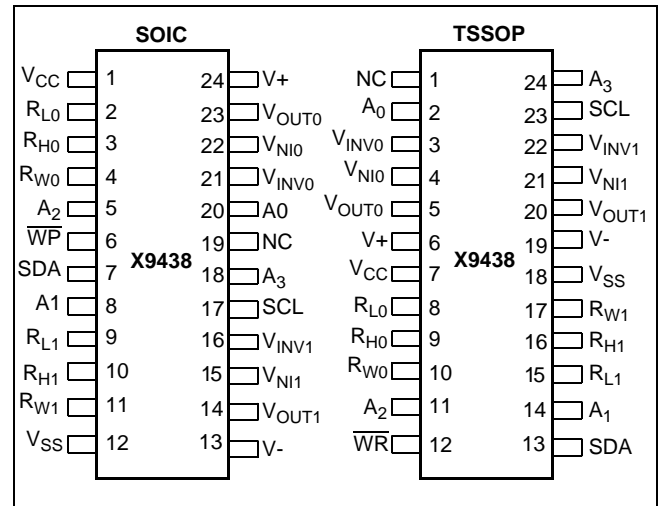
**Analog Supplies V+, V-**

The analog supplies V+, V- are the supply voltages for the XDCP analog section and the operational amplifiers.

**System Supply V<sub>CC</sub> and Ground V<sub>SS</sub>.**

The system supply V<sub>CC</sub> and its reference V<sub>SS</sub> is used to bias the interface and control circuits.

**PIN CONFIGURATION**



**PIN NAMES**

Symbol	Description
SCL	Serial Clock
SDA	Serial Data
A <sub>0</sub> - A <sub>3</sub>	Device Address
R <sub>H0</sub> - R <sub>H1</sub> , R <sub>L0</sub> - R <sub>L1</sub>	Potentiometers (terminal equivalent)
R <sub>W0</sub> - R <sub>W1</sub>	Potentiometers (wiper equivalent)
V <sub>NI(0,1)</sub> , V <sub>INV(0,1)</sub>	Amplifier Input Voltages
V <sub>OUT0</sub> , V <sub>OUT1</sub>	Amplifier Outputs
WP	Hardware Write Protection
V+, V-	Analog and Voltage Amplifier Supplies
V <sub>CC</sub>	System/Digital Supply Voltage
V <sub>SS</sub>	System Ground
NC	No Connection

## PRINCIPLES OF OPERATION

The X9438 is an integrated microcircuit incorporating two resistor arrays, two operational amplifiers and their associated registers and counters; and the serial interface logic providing direct communication between the host and the digitally controlled potentiometers and operational amplifiers.

### Serial Interface

The X9438 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9438 will be considered a slave device in all applications.

### Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods ( $t_{LOW}$ ). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

### Start Condition

All commands to the X9438 are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH ( $t_{HIGH}$ ). The X9438 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

### Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

### Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data.

The X9438 will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9438 will respond with a final acknowledge.

### Operational Amplifier

The voltage operational amplifiers are CMOS rail-to-rail output general purpose amplifiers. They are designed to operate from dual ( $\pm$ ) power supplies. The amplifiers may be configured like any standard amplifier. All pins are externally available to allow connections with the potentiometers or as stand alone amplifiers.

### Potentiometer/Array Description

The X9438 is comprised of two resistor arrays and two operational amplifiers. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (RH and RL inputs).

At both ends of each array and between each resistor segment is a CMOS switch connected to the wiper ( $R_W$ ) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by a volatile wiper counter register (WCR). The six bits of the WCR are decoded to select, and enable, one of sixty-four switches.

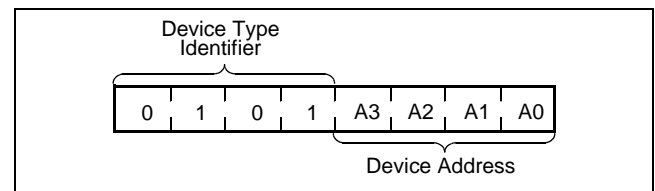
The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and the WCR can be read and written by the host system.

## INSTRUCTIONS AND PROGRAMMING

### Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 1). For the X9438 this is fixed as 0101[B].

**Figure 1. Address/Identification Byte Format**

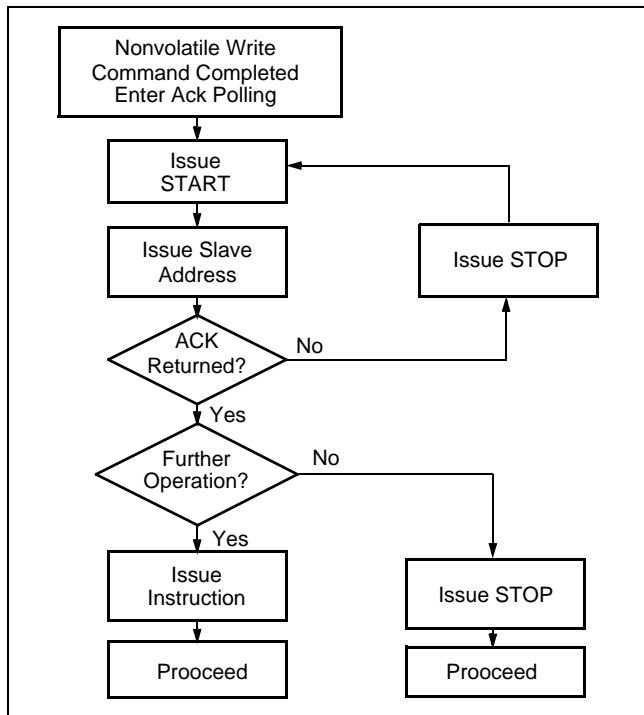


The next four bits of the slave address are the device address. The physical device address is defined by the state of the A<sub>0</sub> - A<sub>3</sub> inputs. The X9438 compares the serial data stream with the address input state; a successful compare of all four address bits is required for the X9438 to respond with an acknowledge. The A<sub>0</sub> - A<sub>3</sub> inputs can be actively driven by CMOS input signals or tied to V<sub>CC</sub> or V<sub>SS</sub>.

**Acknowledge Polling**

The disabling of the inputs, during the internal non-volatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the non-volatile write command the X9438 initiates the internal write cycle. ACK polling (Flow 1) can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9438 is still busy with the write operation no ACK will be returned. If the X9438 has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

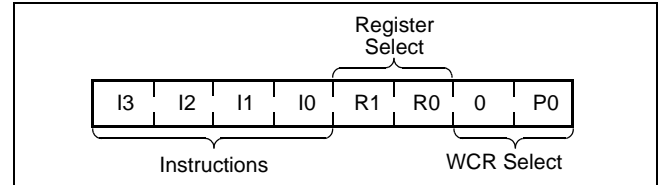
**Flow 1. ACK Polling Sequence**



**Instruction Structure**

The byte following the address contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of the two pots and when applicable they point to one of the four WCRs associated data registers. The format is shown below in Figure 2.

**Figure 2. Instruction Byte Format**



The four high order bits define the instruction. The next two bits (R1 and R0) select one of the two registers that is to be acted upon when a register oriented instruction is issued. The last bit (P0) selects which one of the two potentiometers is to be affected by the instruction.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the wiper counter register and one of the data registers. A transfer from a data register to a wiper counter register is essentially a write to a static RAM. The response of the wiper to this action will be delayed t<sub>WRL</sub>. A transfer from the wiper counter register (current wiper position) to a data register is a write to non-volatile memory and takes a minimum of t<sub>WR</sub> to complete. The transfer can occur between one of the two potentiometers and one of its associated registers; or it may occur globally, wherein the transfer occurs between all of the potentiometers and one of their associated registers.

Four instructions require a three-byte sequence to complete. The basic sequence is illustrated in Figure 4. These instructions transfer data between the host and the X9438; either between the host and one of the data registers or directly between the host and the wiper counter and analog control registers. These instructions are: 1) Read Wiper Counter Register or read the current wiper position of the selected pot, 2) Write Wiper Counter Register, i.e. change current wiper position of the selected pot; 3) Read Data Register, read the contents of the selected non-volatile register; 4) Write Data Register, write a new value to the selected data register. The bit structures of the instructions are shown in Figure 6.

Figure 3. Two-Byte Command Sequence

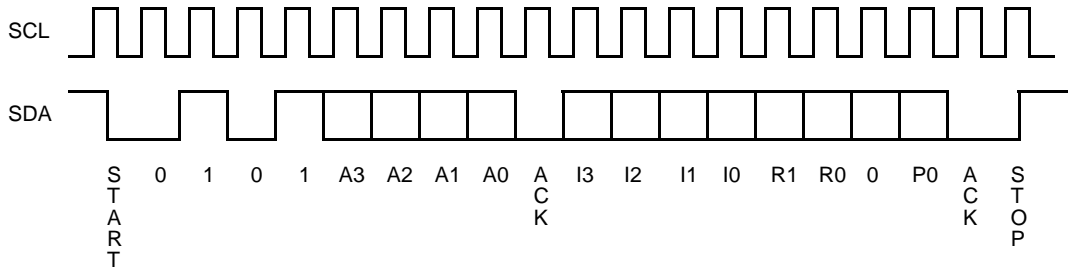
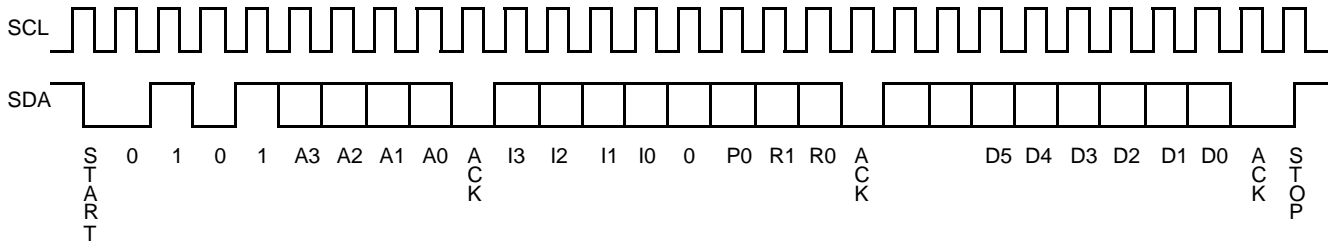


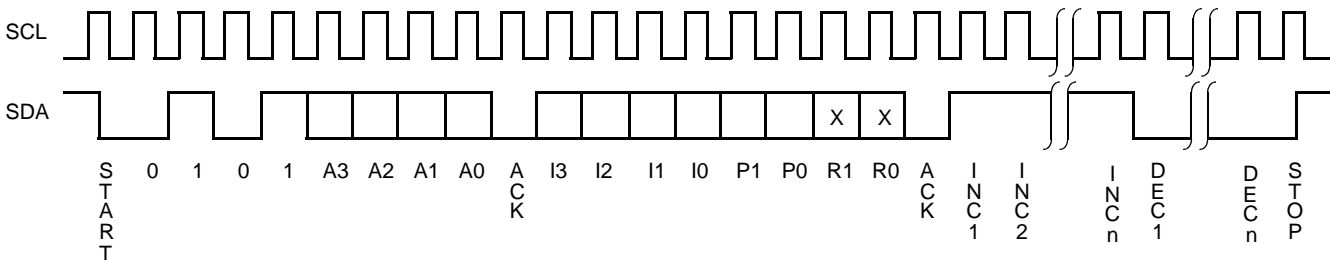
Figure 4. Three-Byte Command Sequence



The Increment/Decrement command is different from the other commands. Once the command is issued and the X9438 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host. For each SCL clock pulse

( $t_{HIGH}$ ) while SDA is HIGH, the selected wiper will move one resistor segment towards the  $V_H$  terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the  $V_L$  terminal. A detailed illustration of the sequence for this operation is shown in Figure 5.

Figure 5. Increment/Decrement Command Sequence



**Figure 6. Instruction Set**

**Read Wiper Counter Register (WCR)**

Read the contents of the Wiper Counter Register P<sub>0</sub>.

START	device type identifier				device addresses				SACK	instruction opcode				WCR addresses				SACK	register data (sent by slave on SDA)								MACK	STOP																	
	0	1	0	1	A3	A2	A1	A0		1	0	0	1	0	0	0	P0		0	0	D5	D4	D3	D2	D1	D0																			
A	0	1	0	1	A	3	A	2	A	1	A	0	S	1	0	0	1	0	0	0	P	0	S	0	0	D	5	D	4	D	3	D	2	D	1	D	0	M	A	C	K	S	T	O	P

P0: 0 - WCR0, 1 - WCR1

**Write Wiper Counter Register (WCR)**

Write new value to the Wiper Counter Register P<sub>0</sub>.

START	device type identifier				device addresses				SACK	instruction opcode				WCR addresses				SACK	register data (sent by master on SDA)								SACK	STOP																	
	0	1	0	1	A3	A2	A1	A0		1	0	1	0	0	0	0	P0		0	0	D5	D4	D3	D2	D1	D0																			
A	0	1	0	1	A	3	A	2	A	1	A	0	S	1	0	1	0	0	0	0	P	0	S	0	0	D	5	D	4	D	3	D	2	D	1	D	0	M	A	C	K	S	T	O	P

P0: 0 - WCR0, 1 - WCR1

**Read Data Register (DR)**

Read the contents of the Register pointed to by P<sub>0</sub> and R<sub>1</sub> - R<sub>0</sub>.

START	device type identifier				device addresses				SACK	instruction opcode				WCR/DR addresses				SACK	register data (sent by master on SDA)								MACK	STOP																			
	0	1	0	1	A3	A2	A1	A0		1	0	1	1	R1	R0	0	P0		0	0	D5	D4	D3	D2	D1	D0																					
A	0	1	0	1	A	3	A	2	A	1	A	0	S	1	0	1	1	R	1	R	0	0	P	0	S	0	0	D	5	D	4	D	3	D	2	D	1	D	0	M	A	C	K	S	T	O	P

R1 R0: 00 - R0, 10 - R1  
01 - R2, 11 - R3

**Write Data Register (DR)**

Write new value to the Register pointed to by P<sub>0</sub> and R<sub>1</sub> - R<sub>0</sub>.

START	device type identifier				device addresses				SACK	instruction opcode				WCR/DR addresses				SACK	register data (sent by master on SDA)								SACK	STOP																				
	0	1	0	1	A3	A2	A1	A0		1	1	0	0	R1	R0	0	P0		0	0	D5	D4	D3	D2	D1	D0																						
A	0	1	0	1	A	3	A	2	A	1	A	0	S	1	1	0	0	R	1	R	0	0	P	0	S	0	0	D	5	D	4	D	3	D	2	D	1	D	0	M	A	C	K	S	T	O	P	HIGH-VOLTAGE WRITE CYCLE

**Definitions:**

SACK - Slave acknowledge, MACK - Master acknowledge, I/D - Increment/Decrement (1/0), R - Register, P - Potentiometer

Figure 6. Instruction Set (continued)

**Transfer Data Register to Wiper Counter Register**

Transfer the contents of the Register pointed to by R<sub>1</sub> - R<sub>0</sub> to the WCR pointed to by P<sub>0</sub>.

S T A R T	device type identifier				device addresses				S A C K	instruction opcode				WCR/DR addresses				S A C K	S T O P
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		1	1	0	1	R <sub>1</sub>	R <sub>0</sub>	0	P <sub>0</sub>		
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		1	1	0	1	R <sub>1</sub>	R <sub>0</sub>	0	P <sub>0</sub>		

**Transfer Wiper Counter Register to Data Register**

Transfer the contents of the WCR pointed to by P<sub>0</sub> to the Register pointed to by R<sub>1</sub> - R<sub>0</sub>.

S T A R T	device type identifier				device addresses				S A C K	instruction opcode				WCR/DR addresses				S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		1	1	1	0	R <sub>1</sub>	R <sub>0</sub>	0	P <sub>0</sub>			
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		1	1	1	0	R <sub>1</sub>	R <sub>0</sub>	0	P <sub>0</sub>			

**Global Transfer Data Register to Wiper Counter Register**

Transfer the contents of all four Data Registers pointed to by R<sub>1</sub> - R<sub>0</sub> to their respective WCR.

S T A R T	device type identifier				device addresses				S A C K	instruction opcode				DR addresses				S A C K	S T O P
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		0	0	0	1	R <sub>1</sub>	R <sub>0</sub>	0	0		
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		0	0	0	1	R <sub>1</sub>	R <sub>0</sub>	0	0		

**Global Transfer Wiper Counter Register to Data Register**

Transfer the contents of all WCRs to their respective data Registers pointed to by R<sub>1</sub> - R<sub>0</sub>.

S T A R T	device type identifier				device addresses				S A C K	instruction opcode				DR addresses				S A C K	S T O P	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		1	0	0	0	R <sub>1</sub>	R <sub>0</sub>	0	0			
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		1	0	0	0	R <sub>1</sub>	R <sub>0</sub>	0	0			

**Increment/Decrement Wiper Counter Register**

Enable Increment/decrement of the WCR pointed to by P<sub>0</sub>.

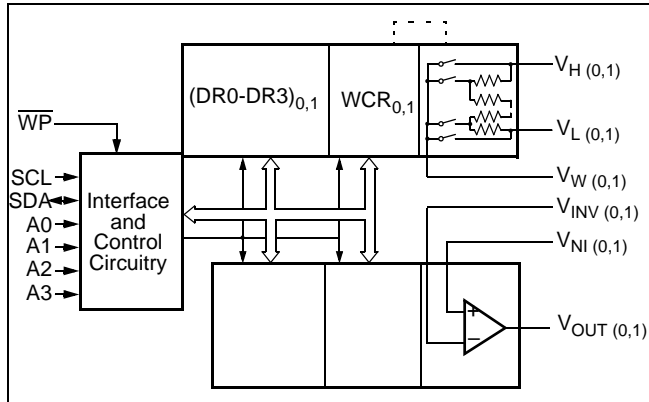
S T A R T	device type identifier				device addresses				S A C K	instruction opcode				WCR addresses				increment/decrement (sent by master on SDA)				S T O P			
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		0	0	1	0	0	0	0	P <sub>0</sub>	I/D	I/D	.	.		.	.	I/D
	0	1	0	1	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>		0	0	1	0	0	0	0	P <sub>0</sub>	I/D	I/D	.	.	.	.	I/D	I/D

P<sub>0</sub>: 0 or 1 only.

**REGISTER OPERATION**

Both digitally controlled potentiometers share the serial interface and share a common architecture. Each potentiometer is associated with a Wiper Counter Register (WCR), and four Data Registers. Figure 7 illustrates the control, registers, and system features of the device.

**Figure 7. System Block Diagram**



**Wiper Counter (WCR) and Analog Control Registers (ACR)**

The X9438 contains two wiper counter registers, one for each XDCCP. The wiper counter register is equivalent to a serial-in, parallel-out counter, with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the wiper counter register can be altered in four ways: it may be written directly by the host via the write WCR Instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers (DR) via the XFR data register instruction (parallel load); it can be modified one step at a time by the increment/decrement instruction (WCR only). Finally, it is loaded with the contents of its data register zero (R0) upon power-up.

The wiper counter register is a volatile register; that is, its contents are lost when the X9438 is powered-down. Although the registers are automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

**Data Registers (DR)**

Each potentiometer has four non-volatile data registers (DR). These can be read or written directly by the host and data can be transferred between any of the four data registers and the WCR. It should be noted all operations changing data in one of these registers is a non-volatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could store system parameters or user preference data.

**REGISTER DESCRIPTIONS AND MEMORY MAP**

**Memory Map**

<b>WCRO</b>	<b>WCR1</b>
DR0	DR0
DR1	DR1
DR2	DR2
DR3	DR3

**Wiper Counter Register (WCR)**

<b>0</b>	<b>0</b>	<b>WP5</b>	<b>WP4</b>	<b>WP3</b>	<b>WP2</b>	<b>WP1</b>	<b>WP0</b>
		(volatile)					(LSB)

WP0-WP5 identify wiper position.

**Data Registers (DR, R0 - R3)**

Wiper Position or User Data (Nonvolatile)
--



**ABSOLUTE MAXIMUM RATINGS**

Temperature under bias ..... -65°C to +135°C  
 Storage temperature ..... -65°C to +150°C  
 Voltage on SDA, SCL or any address  
   input with respect to V<sub>SS</sub> ..... -1V to +7V  
 Voltage on any V+ (referenced to V<sub>SS</sub>) ..... +7V  
 Voltage on any V- (referenced to V<sub>SS</sub>) ..... -7V  
 (V+) - (V-) ..... 10V  
 Any R<sub>H</sub> ..... V+  
 Any R<sub>L</sub> ..... V-  
 Lead temperature (soldering, 10 seconds) ..... 300°C

**COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C

Device	Supply Voltage (V <sub>CC</sub> ) Limits
X9438	5V ±10%
X9438-2.7	2.7V to 5.5V

**POTENTIOMETER CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
R <sub>TOTAL</sub>	End to end resistance	-20		+20	%	
	Power rating			50	mW	25°C, each pot
I <sub>W</sub>	Wiper current	-3		+3	mA	
R <sub>W</sub>	Wiper resistance		40	100	Ω	V <sub>CC</sub> = 5V, Wiper Current = 3mA
			100	250	Ω	V <sub>CC</sub> = 2.7, Wiper Current = 1mA
V <sub>V+</sub>	Voltage on V+ pin	X9438	+4.5	+5.5	V	
		X9438-2.7	+2.7	+5.5		
V <sub>V-</sub>	Voltage on V- pin	X9438	-5.5	-4.5	V	
		X9438-2.7	-5.5	-2.7		
V <sub>TERM</sub>	Voltage on any R <sub>H</sub> or R <sub>L</sub> pin	V-		V+	V	
	Noise		-100		dBv	Ref: 1V
	Resolution <sup>(4)</sup>		1.6		%	
	Absolute linearity <sup>(1)</sup>	-1		+1	MI <sup>(3)</sup>	V <sub>w(n)(actual)</sub> - V <sub>w(n)(expected)</sub>
	Relative linearity <sup>(2)</sup>	-0.2		+0.2	MI <sup>(3)</sup>	V <sub>w(n+1)</sub> - [V <sub>w(n)</sub> + MI]
	Temperature coefficient of R <sub>TOTAL</sub>		±300		ppm/°C	
	Ratiometric temperature coefficient			±20	ppm/°C	

- Notes: (1) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.  
 (2) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.  
 (3) MI = RTOT/63 or (R<sub>H</sub> - R<sub>L</sub>)/63, single pot (= LSB)  
 (4) Individual array resolutions

**AMPLIFIER ELECTRICAL CHARACTERISTICS**

(Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Condition	Industrial			Commercial			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V <sub>OS</sub>	Input offset voltage	V+/V- ±3V to ±5V		1	3		1	2	mV
TC <sub>VOS</sub>	Input offset voltage temp. coefficient	V+/V- ±3V to ±5V		-10			-10		µV/°C
I <sub>B</sub>	Input bias current	V+/V- ±3V to ±5V		50			50		pA
I <sub>OS</sub>	Input offset current	V+/V- ±3V to ±5V		25			25		pA
CMRR	Common mode rejection ratio	V <sub>CM</sub> = -1V to +1V	70			70			dB
PSRR	Power supply rejection ratio	V+/V- ±3V to ±5V	70			70			dB
V <sub>CM</sub>	Input common mode voltage range	T <sub>J</sub> = 25°C	V-		V+	V-		V+	V
A <sub>V</sub>	Large signal voltage gain	V <sub>O</sub> = -1V to +1V	30	50		30	50		V/mV
V <sub>O</sub>	Output voltage swing	V- V+	+0.1		-0.15	+0.1		-0.15	V V
I <sub>O</sub>	Output current	V+/V- = ±5.5V V+/V- = ±3.3V	50 30			50 30			mA mA
I <sub>S</sub>	Supply current	V+/V- = ±5.0V			3			3	mA
		V+/V- = ±3.0V			1.5			1.5	mA
GB	Gain-bandwidth prod	R <sub>L</sub> = 100k, C <sub>L</sub> = 50pf		1.0			1.0		MHz
SR	Slew rate	R <sub>L</sub> = 100k, C <sub>L</sub> = 50pf		1.5			1.5		V/µsec
Φ <sub>M</sub>	Phase margin	R <sub>L</sub> = 100k, C <sub>L</sub> = 50pf		80			80		Deg.

V+ and V- (±5V to ±3V) are the amplifier power supplies. The amplifiers are specified with dual power supplies. V<sub>CC</sub> and V<sub>SS</sub> is the logic supply. All ratings are over the temperature range for the Industrial (-40 to +85°C) and Commercial (0 to 70°C) versions of the part unless specified differently.

**SYSTEM/DIGITAL D.C. OPERATING CHARACTERISTICS**

(Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits				Test Conditions
		Min.	Typ.	Max.	Unit	
I <sub>CC</sub>	V <sub>CC</sub> supply current (active)			400	µA	f <sub>SCL</sub> = 400kHz, SDA = Open, Other Inputs = V <sub>SS</sub>
I <sub>SB</sub>	V <sub>CC</sub> current (standby)			1	µA	SCL = SDA = V <sub>CC</sub> , Addr. = V <sub>SS</sub>
I <sub>LI</sub>	Input leakage current			10	µA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>LO</sub>	Output leakage current			10	µA	V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>
V <sub>IH</sub>	Input HIGH voltage	V <sub>CC</sub> × 0.7		V <sub>CC</sub> + 0.5	V	
V <sub>IL</sub>	Input LOW voltage	-0.5		V <sub>CC</sub> × 0.1	V	
V <sub>OL</sub>	Output LOW voltage			0.4	V	I <sub>OL</sub> = 3mA

**ENDURANCE AND DATA RETENTION**

Parameter	Min.	Unit
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	Years

**CAPACITANCE**

Symbol	Test	Typical	Unit	Test Conditions
$C_{I/O}$	Input/output capacitance (SDA)	8	pF	$V_{I/O} = 0V$
$C_{IN}$	Input capacitance (A0, A1, A2, A3, and SCL)	6	pF	$V_{IN} = 0V$
$C_L   C_H   C_W$	Potentiometer capacitance	10/10/25	pF	See SPICE Model

**POWER-UP TIMING AND SEQUENCE**

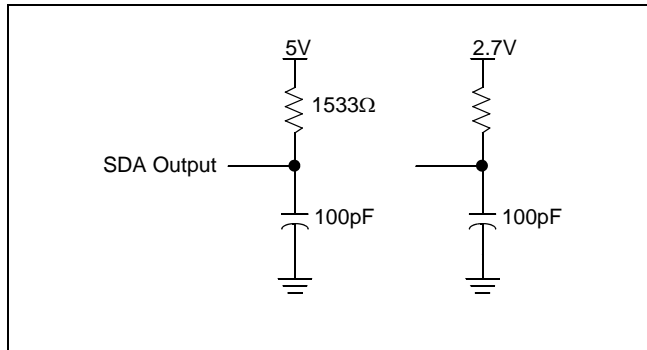
Power-up sequence <sup>(1)</sup> : (1) $V_{CC}$ (2) $V+$ and $V-$
Power-down sequence: no limitation

**A.C. TEST CONDITIONS**

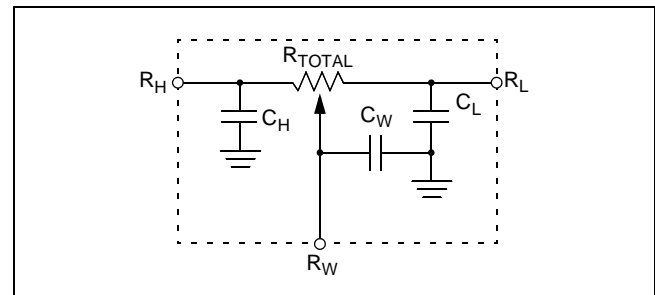
Input pulse levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input rise and fall times	10ns
Input and output timing level	$V_{CC} \times 0.5$

Note: (1) Applicable to recall and power consumption applications

**EQUIVALENT A.C. LOAD CIRCUIT**

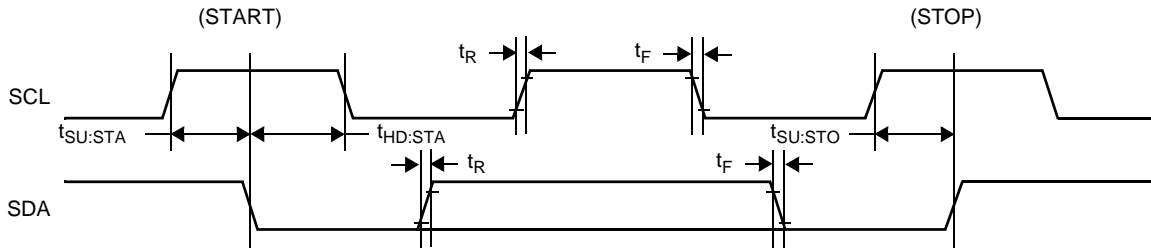


**SPICE Macro Model**

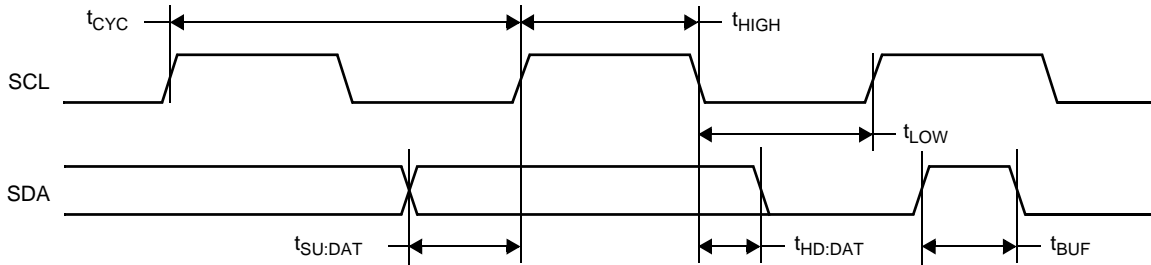


TIMING DIAGRAMS

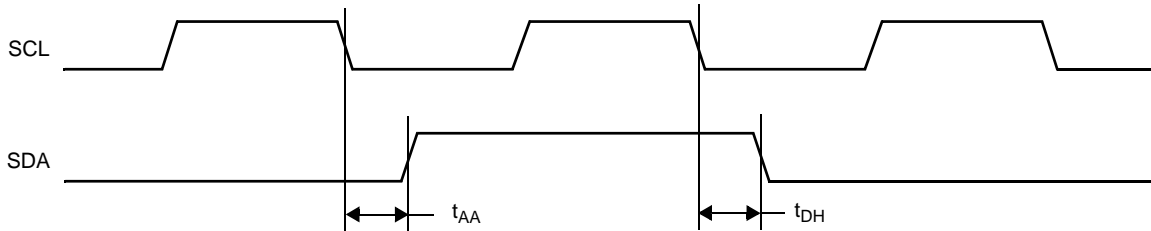
START and STOP Timing



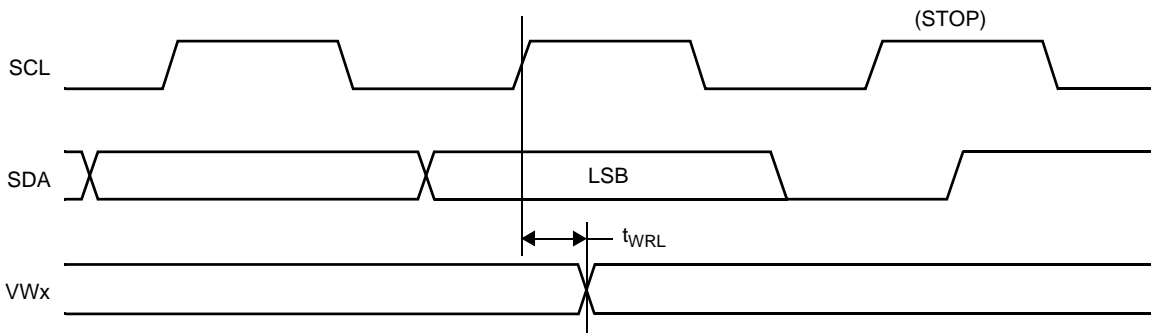
Input Timing



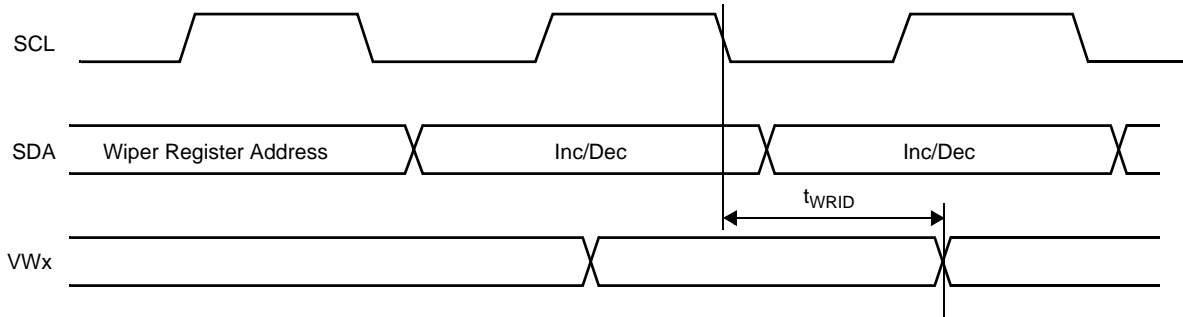
Output Timing



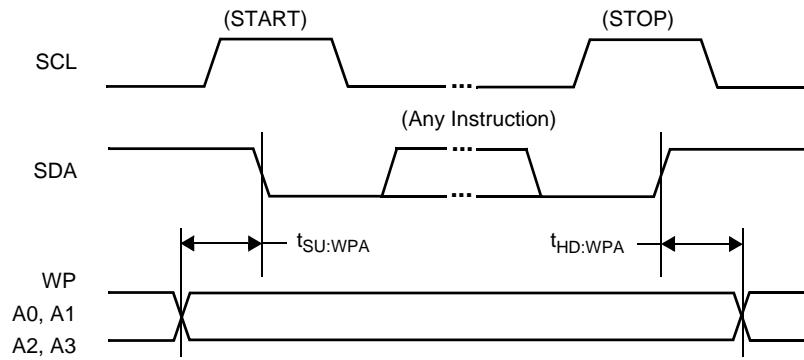
DCP Timing (for All Load Instructions)



**DCP Timing (for Increment/Decrement Instruction)**



**Write Protect and Device Address Pins Timing**



## AC TIMING

Symbol	Parameter	Min.	Max.	Unit
$f_{SCL}$	Clock frequency		400	kHz
$t_{CYC}$	Clock cycle time	2500		ns
$t_{HIGH}$	Clock high time	600		ns
$t_{LOW}$	Clock low time	1300		ns
$t_{SU:STA}$	Start setup time	600		ns
$t_{HD:STA}$	Start hold time	600		ns
$t_{SU:STO}$	Stop setup time	600		ns
$t_{SU:DAT}$	SDA data input setup time	100		ns
$t_{HD:DAT}^{(4)}$	SDA data input hold time	0/30		ns
$t_R$	SCL and SDA rise time		300	ns
$t_F$	SCL and SDA fall time		300	ns
$t_{AA}$	SCL low to SDA data output valid time	100	900	ns
$t_{DH}$	SDA data output hold time	50		ns
$T_I$	Noise suppression time constant at SCL and SDA inputs	50		ns
$t_{BUF}$	Bus free time (Prior to Any Transmission)	1300		ns
$t_{SU:WPA}$	$\overline{WP}$ , A0, A1, A2 and A3 setup time	0		ns
$t_{HD:WPA}$	$\overline{WP}$ , A0, A1, A2 and A3 hold time	0		ns

Note: (4)  $V_{CC} = 5V/2.7V$

## HIGH-VOLTAGE WRITE CYCLE TIMING

Symbol	Parameter	Typ.	Max.	Unit
$t_{WR}$	High-voltage write cycle time (store instructions)	5	10	ms

## DCP TIMING

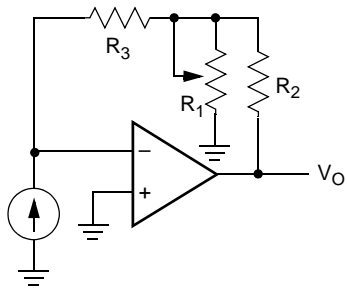
Symbol	Parameter	Min.	Max.	Unit
$t_{WRL}$	Wiper response time after instruction issued (All load instructions)		10	$\mu s$

 $V_{CC}$  RAMP (sample tester)

Symbol	Parameter	Typ.	Max.	Unit
$trV_{CC}$	$V_{CC}$ Power-up rate	.2	50	V/ms

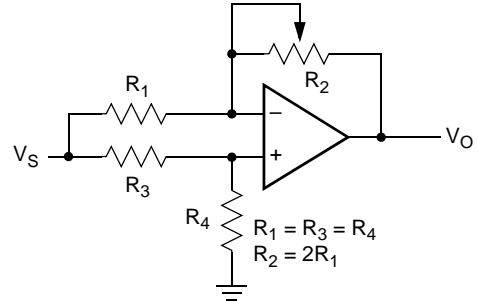
BASIC APPLICATIONS

I to V Converter



$$V_O/I_S = -R_3(1 + R_2/R_1) + R_2$$

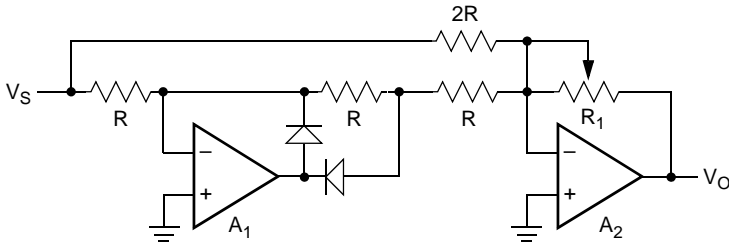
Attenuator



$$V_O = G V_S$$

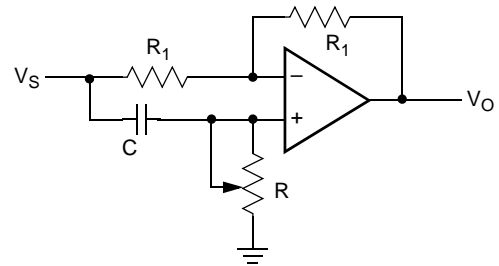
$$-1/2 \leq G \leq +1/2$$

Absolute Value Amplifier with Gain



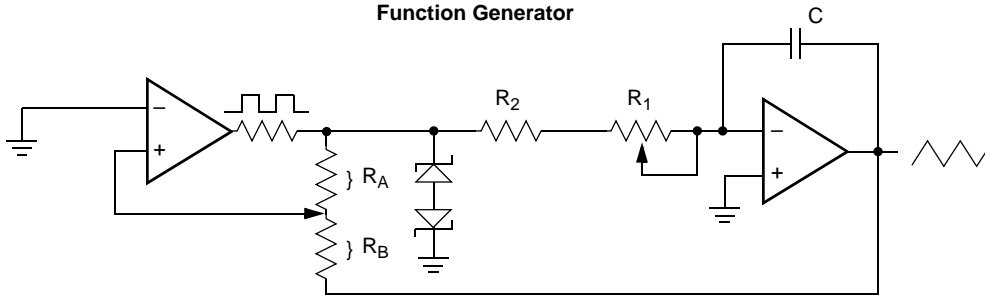
$$V_O = |V_S| \frac{R_1}{R}$$

Phase Shifter



$$\angle V_O/V_S = 180^\circ - 2 \tan^{-1} \omega RC$$

Function Generator

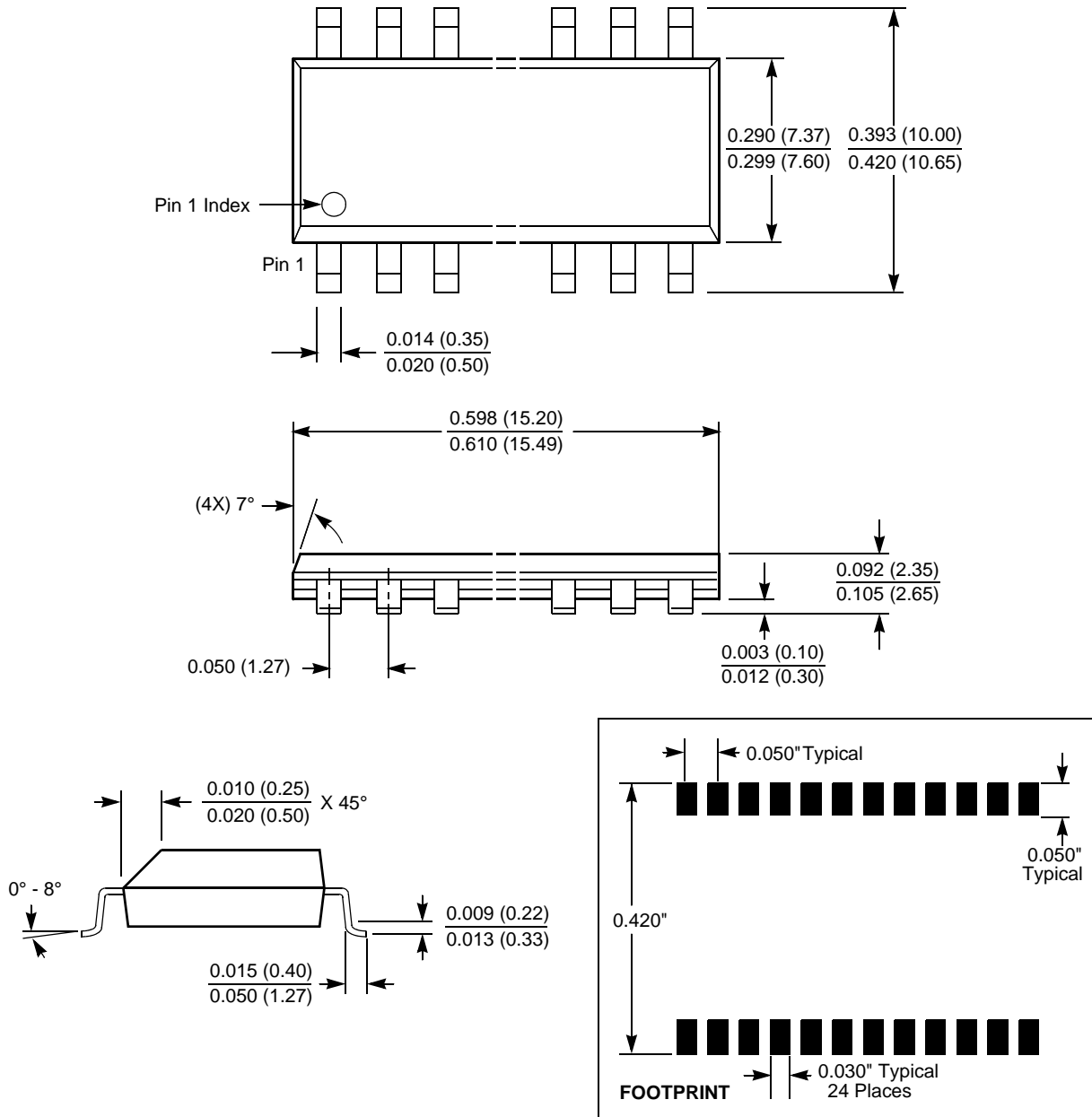


$$\text{frequency} \propto R_1, R_2, C$$

$$\text{amplitude} \propto R_A, R_B$$

PACKAGING INFORMATION

24-Lead Plastic Small Outline Gull Wing Package Type S

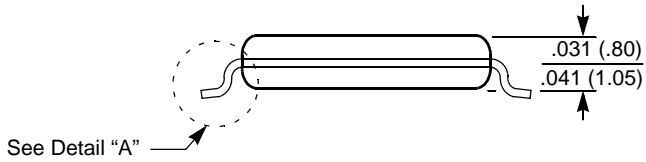
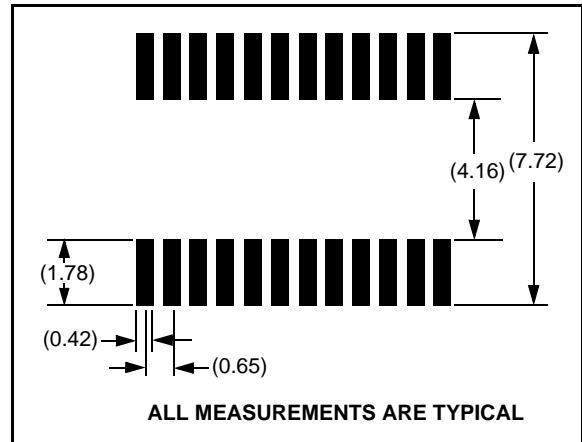
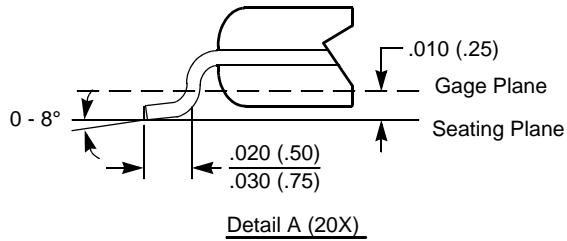
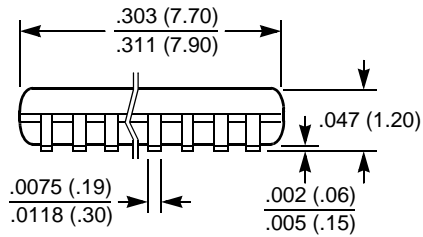
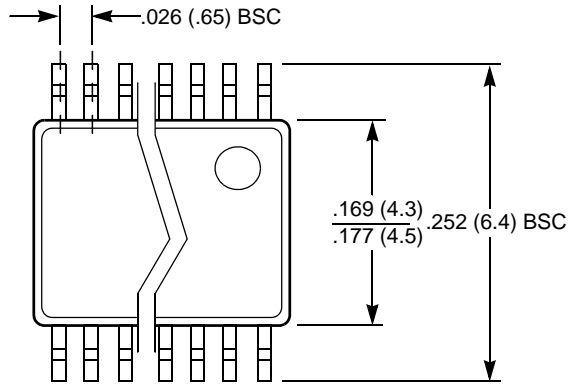


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)



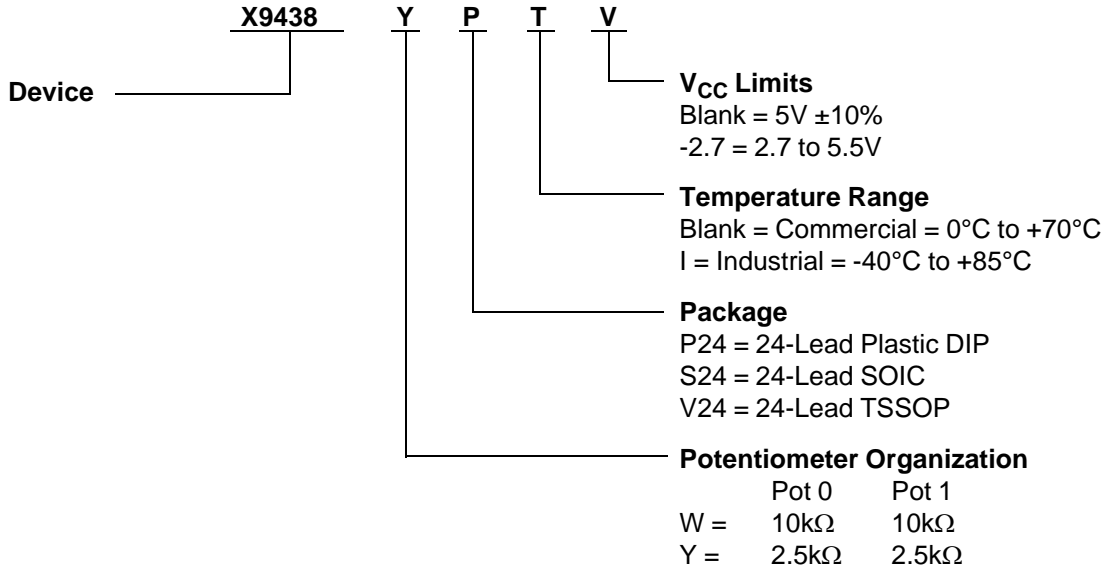
PACKAGING INFORMATION

24-Lead Plastic, TSSOP Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information



All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.  
Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)